1	**1**	**Marks are for AO1 (knowledge)** Instructions are stored in (main) memory; Instructions are fetched, (decoded) and executed (serially) by the processor; Programs can be moved in and out of main memory; **Max 2**	**2**

2	1	**2 marks are for AO1 (knowledge)** Instructions are stored in (main) memory; Instructions are fetched, (decoded) and executed (serially) by the processor; Programs can be moved in and out of main memory; **MAX 2**	2

Qu	Pt	Marking Guidance	Marks
3	1	**Marks are for AO1 (knowledge)** (Machine code) Instructions are stored in (main) memory; Instructions are fetched, (decoded) and executed (serially) by the processor; Programs can be moved in to (and out of) main memory; **Max 2**	2

4 **All marks AO1 (understanding)** **12**

Level	Description	Mark Range
4	A line of reasoning has been followed to produce a coherent, relevant, substantiated and logically structured response. The response covers all three areas indicated in the guidance below and in at least two of these areas there is sufficient detail to show that the student has a good level of understanding. To reach the top of this mark range, a good level of understanding must be shown of all three areas.	10-12
3	A line of reasoning has been followed to produce a coherent, relevant, substantiated and logically structured response which shows a good level of understanding of at least two areas indicated in the guidance below.	7-9
2	A limited attempt has been made to follow a line of reasoning and the response has a mostly logical structure. Either a good level of understanding of one area from the guidance has been shown or a limited understanding of two areas.	4-6
1	A few relevant points have been made but there is no evidence that a line of reasoning has been followed. The points may only relate to one or two of the areas from the guidance or may be made in a superficial way with little substantiation.	1-3

Guidance – Indicative Response

1. Why translation is necessary

Processor can only execute machine code instructions **A.** computer for processor

High-level instructions cannot be executed directly // high-level instructions are not machine code **A.** must be converted to machine code to be executed

NE. "Understand" for "execute".

Good level of understanding = at least one point made

2. Differences between compilation and interpreting

Compiler analyses program as a whole

Interpreter analyses program on a line-by-line basis

Compiler produces object code/executable file/machine code/bytecode

Interpreter calls subroutines within its own code to carry out commands

Compiler will not translate any of the program if it encounters an error

Interpreter translates/executes program until first error is encountered

If (unchanged) program executed twice/multiple times, compiler will only need to translate it once

Interpreter translates a program each time it is executed

Interpreter executes each line immediately after translating it

If student has written about compiler outputting bytecode then: bytecode will later be interpreted // executed by a virtual machine // just-in-time-compiled

Once translated, compiled code does not need the compiler to be present to run

An interpreter must always be present for a program that is interpreted to run

Once compiled, code will only run on one type of processor / virtual machine

Interpreter could translate the same instruction multiple times (eg if it is in a loop)

Good level of understanding = at least four points made

3. How machine code instructions fetched and executed

F-E Stage 1 Fetch:

Contents of Program Counter / PC transferred to Memory Address Register / MAR
R. if implied the instruction is stored in the PC

Address bus used to transfer this address to main memory

Transfer of main memory content uses the data bus

Contents of addressed memory location loaded into the Memory Buffer Register / MBR

Increment (contents of) Program Counter / PC **A**. at any part of fetch process after transferring PC to MAR

Increment Program Counter / PC and fetch instruction simultaneously

Contents of MBR copied to CIR

F-E Stage 2 Decode:

Decode instruction held by the (Current) Instruction Register / (C)IR

The control unit decodes the instruction

Instruction split into opcode and operand

F-E Stage 3 Execute:

If necessary, data is fetched

If necessary, data is stored in memory

The opcode identifies the type of operation/instruction to be performed (by the processor)

Result (may be) stored in register/accumulator

The operation (identified by the opcode) is performed by the processor. **A.** ALU

Status register updated

If jump / branch required Program Counter/PC is updated

General:

Instructions will be for program (if compiled) or interpreter (if interpreted)

Good level of understanding = at least five points made and at least two of the three stages of the F-E cycle are covered.

Qu	Pt	Marking guidance	Total marks
5	1	**Mark is AO1 (understanding)** **B**; (The computer can only be used with one program) **R.** more than one lozenge shaded	1